AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A channel region of a depletion type lateral field effect transistor, said channel region of a first conductivity type being selectively provided in a semiconductor region of a second conductivity type, and said channel region underlying a gate insulating film,

wherein an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region.

Claim 2 (previously presented): The channel region as claimed in claim 1, wherein said semiconductor region comprises a well region of the second conductivity type selectively provided in a semiconductor substrate of the first conductivity type.

Claim 3 (original): The channel region as claimed in claim 1, wherein said channel region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of said depletion type lateral field effect transistor.

Claim 4 (original): A well region for a depletion type lateral field effect transistor, said well region of a second

conductivity type being selectively provided in a semiconductor substrate, said well region having an upper surface and including an impurity diffused region which is selectively provided in said well region, and said impurity diffused region being doped with an impurity of a first conductivity type which is for adjustment to a threshold voltage of said depletion type lateral field effect transistor,

wherein said upper surface of said impurity diffused region lies at a lower level than said upper surface of said well region.

Claim 5 (previously presented): The well region as claimed in claim 4, wherein said upper surface of said impurity diffused region is bounded with a gate insulating film.

Claims 6 and 7 (canceled).

Claim 8 (original): A depletion type lateral MOS field effect transistor comprising:

a channel region of a first conductivity type being selectively provided in a semiconductor region of a second conductivity type;

source and drain regions of the first conductivity type being selectively provided in said semiconductor region, said channel region being interposed between said source and drain regions;

a gate insulating film extending over said channel region; and

a gate electrode provided on said gate insulating film,

wherein an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region.

Claim 9 (original): The channel region as claimed in claim 8, wherein said semiconductor region comprises a well region selectively provided in an epitaxial layer of the first conductivity type, and said epitaxial layer overlying a semiconductor substrate of the first conductivity type.

Claim 10 (original): The channel region as claimed in claim 8, wherein said channel region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of said depletion type lateral field effect transistor.

Claim 11 (currently amended): A semiconductor wafer including:

an impurity diffused region of a first conductivity type comprising a channel region being selectively provided in a semiconductor region of a second conductivity type; and

an oxide film overlying said impurity diffused region ~~with an upper surface of the semiconductor region being exposed~~

~~at an upper surface of said semiconductor wafer on each end of the oxide film~~, wherein,

an interface of said impurity diffused region to said oxide film lies at a lower level than ~~the~~ an upper surface of said semiconductor wafer, and

said semiconductor region comprises a well region of the second conductivity type selectively provided in a semiconductor substrate of the first conductivity type.

Claim 12 (canceled).

Claim 13 (original): The semiconductor wafer as claimed in claim 11, wherein said channel region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of a depletion type lateral field effect transistor.

Claim 14 (original): The semiconductor wafer as claimed in claim 11, wherein said oxide film has a thickness of at least 5000 angstroms.

Claims 15-26 (canceled).

Claim 27 (previously presented): The well region as claimed in claim 4, wherein said impurity diffused region forms a channel layer of said depletion type lateral field effect transistor.

Claim 28 (previously presented): A semiconductor wafer comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial layer of the first conductivity type overlying said semiconductor substrate;

a well region of a second conductivity type selectively provided in said epitaxial layer; and

an impurity diffused channel region being selectively provided in said well region, and said impurity diffused channel region being doped with an impurity of the first conductivity type which is for adjustment to a threshold voltage of a depletion type lateral field effect transistor,

wherein said upper surface of said impurity diffused channel region lies at a lower level than said upper surface of said well region.

Claim 29 (previously presented): The semiconductor wafer as claimed in claim 28, wherein said upper surface of said impurity diffused region is bounded with a gate insulating film.

Claim 30 (previously presented): The depletion type lateral MOS field effect transistor of claim 8, wherein,

the channel region, provided in the semiconductor region, comprises throughout the channel region a first concentration of first impurities of the second conductivity type and a higher second concentration of second impurities of the first conductivity type whereby the channel region is of the first conductivity type, and

Claim 33 (previously presented): A lateral field effect transistor, comprising:

an n+-type semiconductor substrate impurity concentration;

an n⁻-type epitaxial layer (2) with a concentration formed over the substrate, the sec being lower than the first concentration;

a p-well region (5) formed in the layer with an uppermost surface of the p-well planar with an uppermost surface of the n⁻-type and

an n-type channel region (6) forme region; and

wherein an uppermost surface of the cl at a lower level than the uppermost surface of t

Claim 34 (previously presented): T claim 33, further comprising:

a gate oxide film extending over the

field oxide films contacting each end film and extending over the p-well;

a source region contacting a first en region, said gate oxide film, and one of said f and

a drain region contacting a second en

the semiconductor region comprises a third concentration of the first impurities of the second conductivity type, the third concentration being higher than the first concentration.

Claim 31 (previously presented): The channel region of claim 1, wherein,

the channel region, provided in the semiconductor region, comprises a first concentration of first impurities of the second conductivity type and a higher second concentration of second impurities of the first conductivity type whereby the channel region is of the first conductivity type, and

the semiconductor region comprises a third concentration of the first impurities of the second conductivity type, the third concentration being higher than the first concentration.

Claim 32 (previously presented): The well region of claim 4, wherein,

the impurity diffused region is a channel region,

the channel region comprises a first concentration of a first impurity of the second conductivity type and a higher second concentration of the impurity of the first conductivity type whereby the channel region is of the first conductivity type, and

the well comprises a third concentration of the first impurity of the second conductivity type, the third concentration being higher than the first concentration.

region, said gate oxide film, and another of said field oxide films.

Claim 35 (previously presented): The transistor of claim 33, wherein,

the gate oxide film extending over the channel region the n-type channel region comprises a low concentration of a p-type impurity and a higher concentration of an n-type impurity, and

the p-well region comprises the p-type impurity.

Claim 36 (previously presented): The transistor of claim 35, wherein a concentration of the p-type impurity in the p-well is higher than the low concentration of the p-type impurity in the n-type channel region.

Claim 37 (previously presented): The transistor of claim 34, wherein,

the gate oxide film extending over the channel region has a thickness of 300 angstroms, and

the field oxide films contacting each end of the gate oxide film have a thickness of at least 5000 angstroms.

Claim 38 (previously presented): The channel region as claimed in claim 2, wherein said well region comprises a planar lower surface along an entire length of the lower surface.

Claim 39 (previously presented): The well region of claim 4, wherein said well region comprises a planar lower surface along an entire length of the lower surface.

Claim 40 (currently amended): The semiconductor wafer as claimed in claim [[12]] 11, wherein said well region comprises a planar lower surface along an entire length of the lower surface.

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Box PG Pub Drawings

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Specification Not in English

6/26/03